

Discussion of  
“A New Approach for Quality Adjusting  
PPI Microprocessors”  
Steven Sawyer and Alvin So

David Byrne\*†

Prepared for the “Research on Income and Wealth” session  
at the 2017 NBER Summer Institute

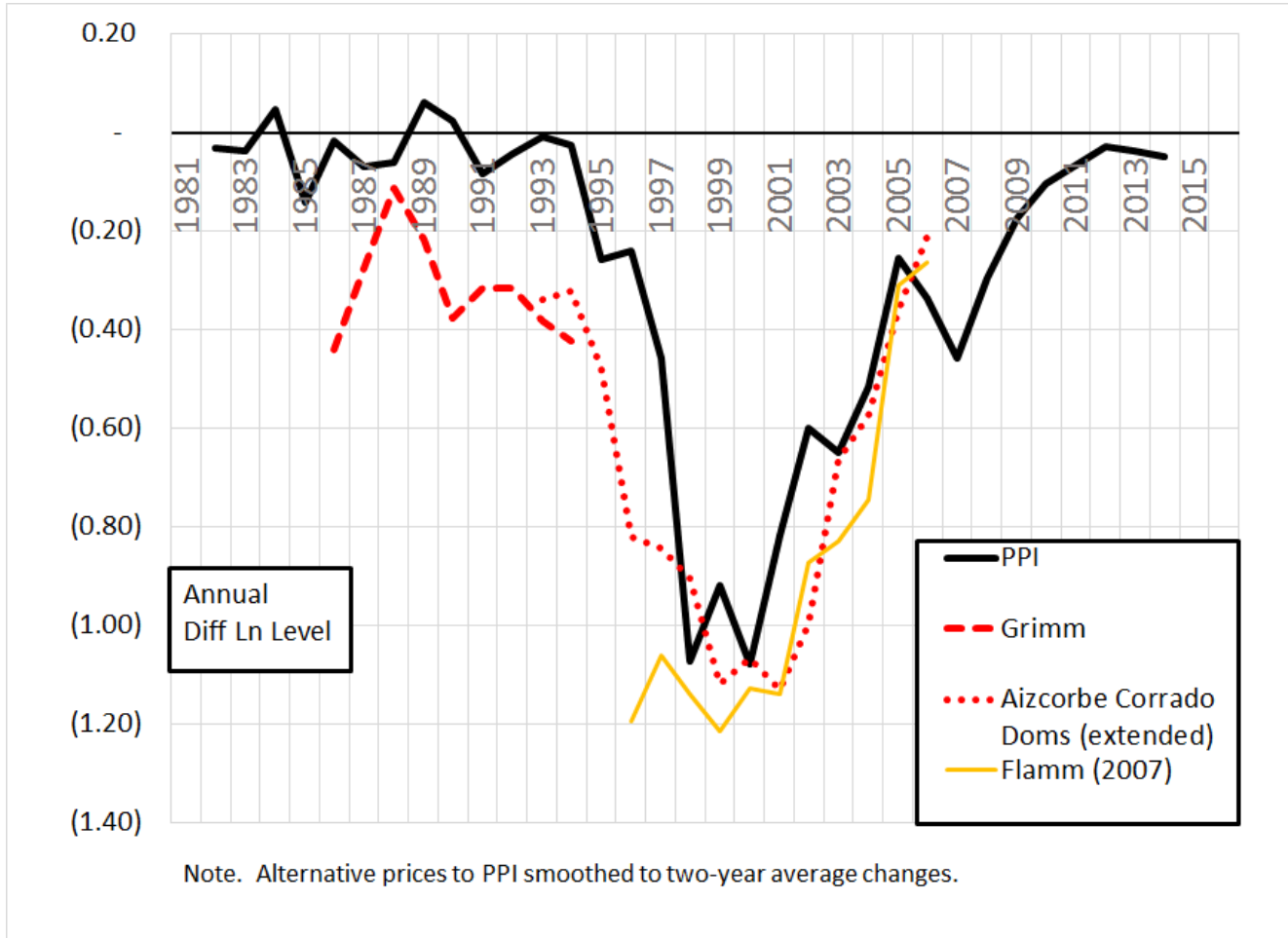
\* Principal Economist, Federal Reserve Board of Governors. [david.m.byrne@frb.gov](mailto:david.m.byrne@frb.gov). These remarks are the opinion of the discussant and do not necessarily reflect the views of the Federal Reserve Board of Governors or other members of the Federal Reserve staff.

† The Bureau of Labor Statistics has not indicated to the discussant that the prices of any specific company are used in the construction of the Producer Price Index.

# Bottom Line

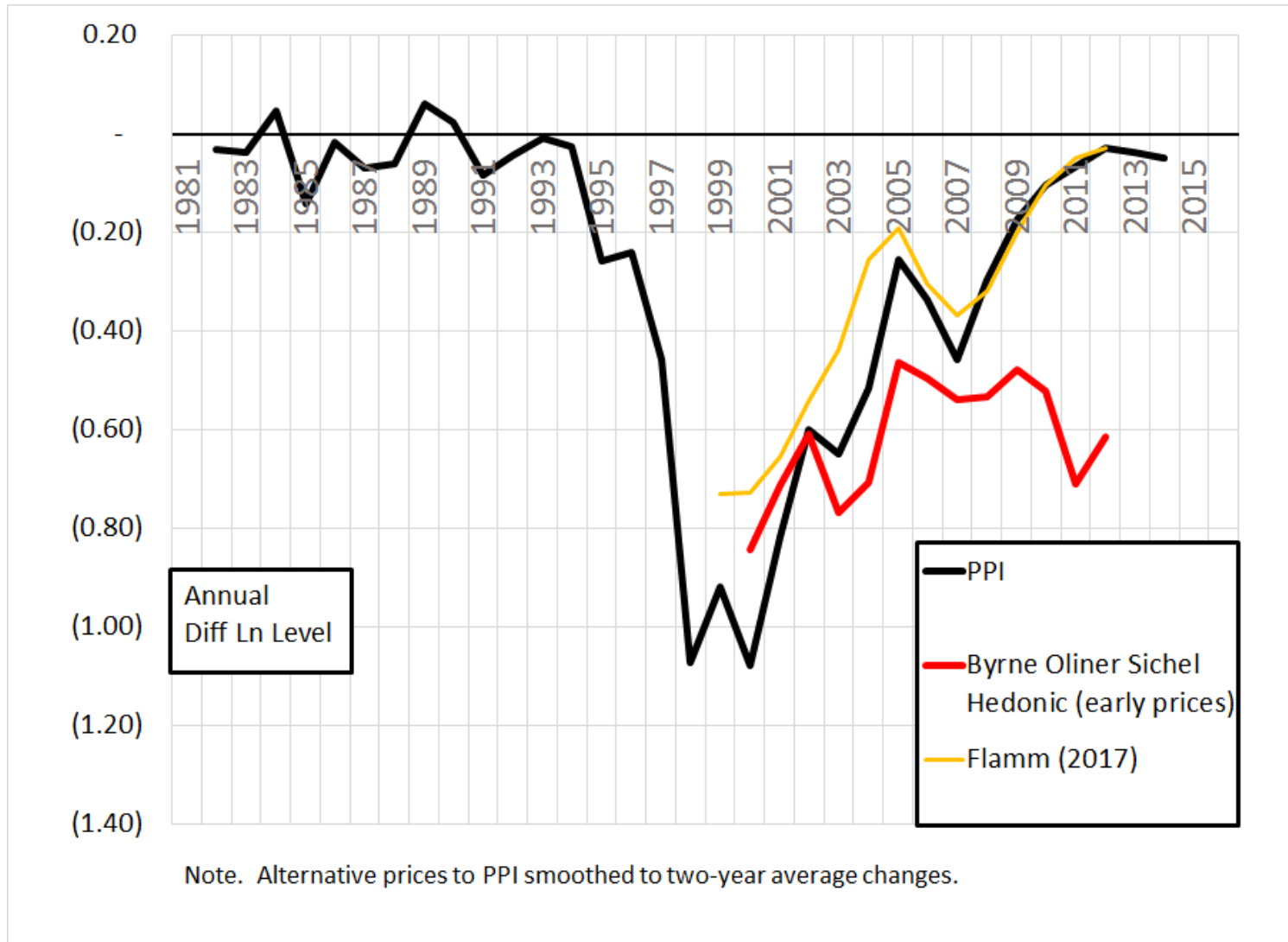
- Admirable effort to tackle a very thorny measurement problem.
- Highly commendable change in PPI methodology
- Room for refinement
  - Prices used
  - Control variables employed
  - Estimation technique
- *Quibbles about interpretation of Byrne-Oliner-Sichel paper, data, and market structure. Mostly delivered offline.*

# History of MPU Price Indexes (1)



- 1981-1997: PPI declines very slowly.
- 1997: Responding to research by BEA & FRB, BLS supplements survey data with price lists published by a non-responding MPU manufacturer with 85% market share. [Presumably Intel]
- 1997-2006: BLS, FRB, and Flamm indexes largely consistent.
- 2006 -2014: PPI returns to slow declines
- March 2015: most recent monthly value of the index.

# History of MPU Price Indexes (2)



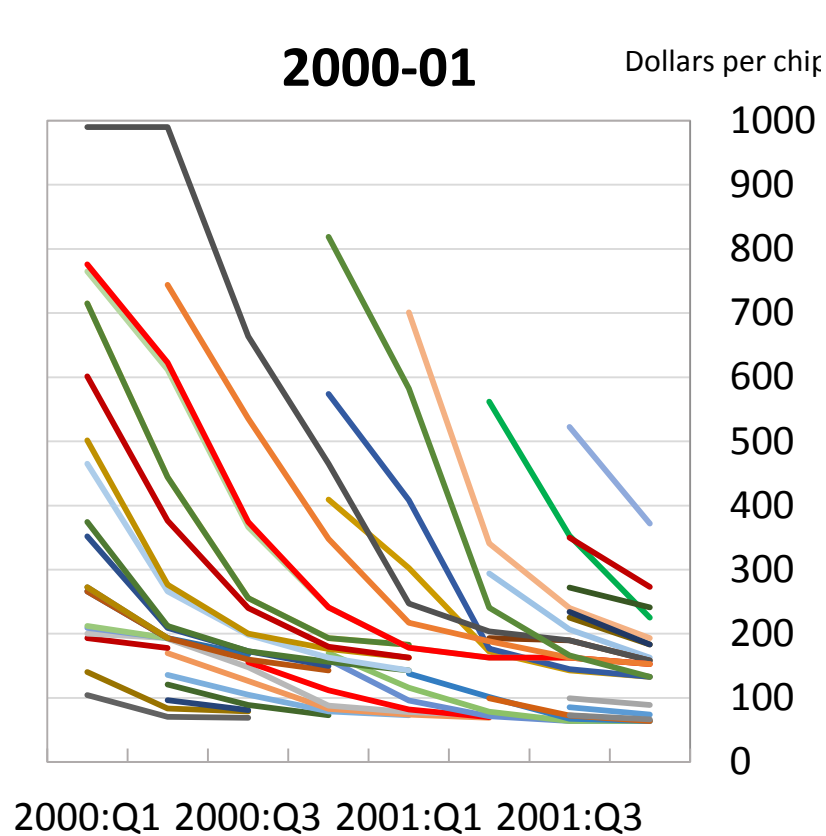
- Byrne, Oliner, Sichel (2017): MPU prices have decline rapidly through 2013.
- Flamm (2017): PPI is correct.
- Consensus: Slowdown
- Debate: Magnitude

# Slowdown Explanations

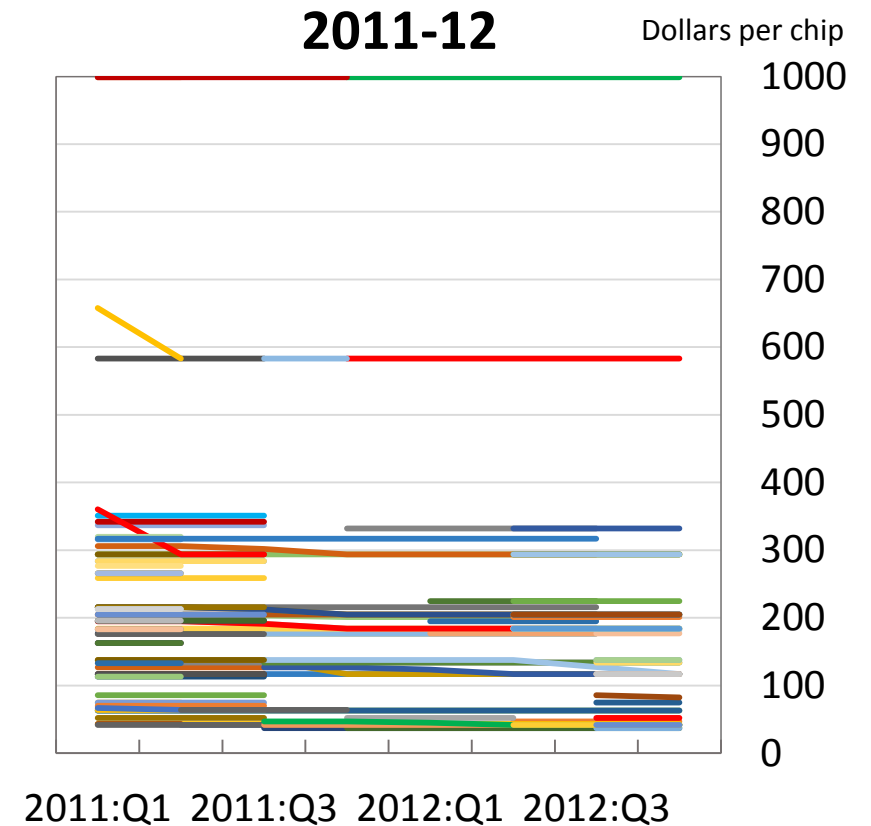
- Technology: Moore's law / heat dissipation / clockspeed
- Market structure: AMD v. Intel
- Structure of the price data
- *All three are true. We'll focus on the price data.*

# Intel Price List Evolution

Price trends for individual MPU models show a stark change in the mid 2000s.



Prior to mid-2000s:  
Price cascade.  
Approach: superlative index.

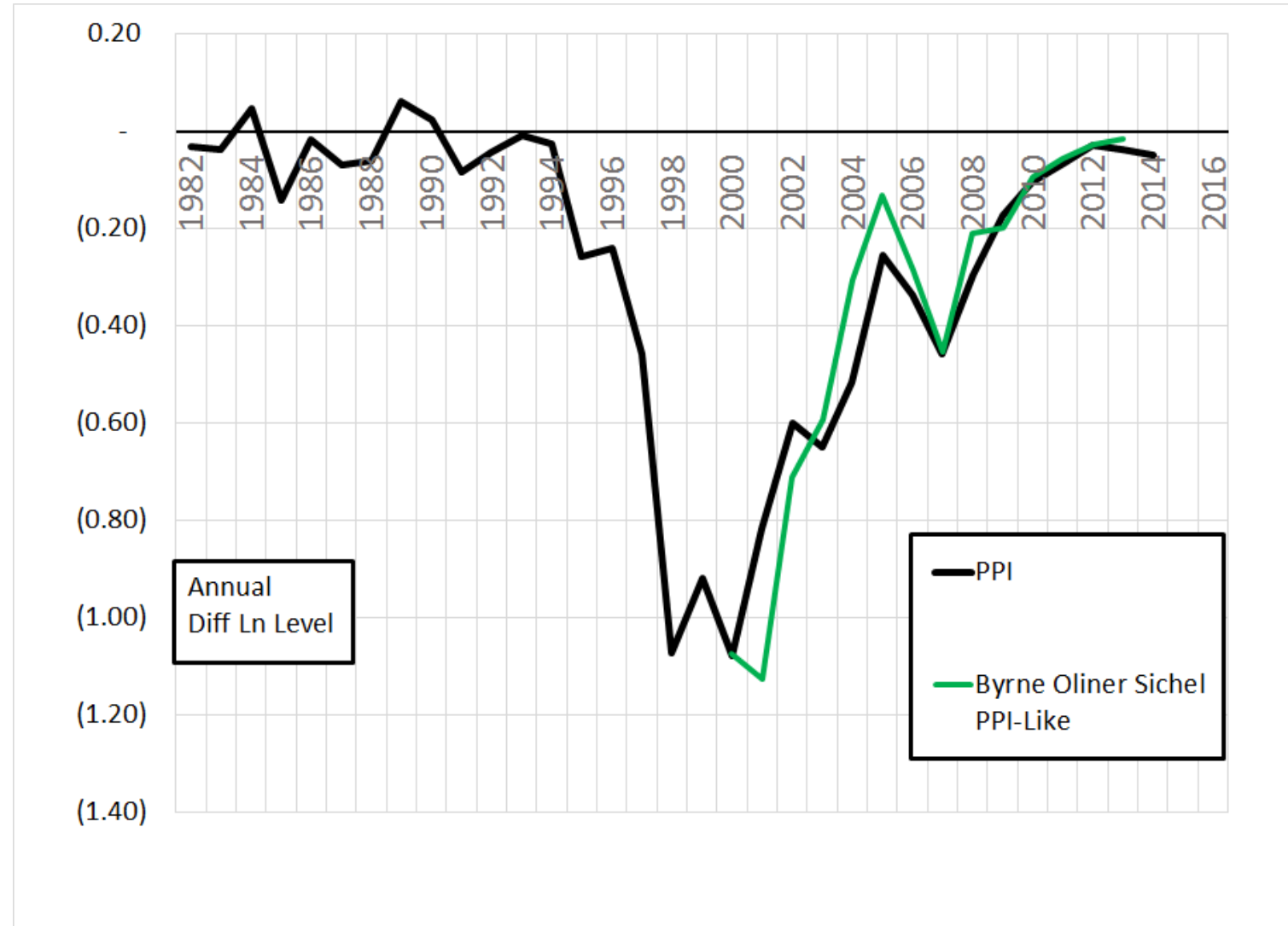


Post mid-2000s:  
**Flatline prices.**  
Best approach: ????

# Matched Model using Intel Price List Data

BOS (2017) construct a “ppi-like” index with these prices that mimics the PPI.

Does this deceleration make sense?



# Contradicted by Price-Performance Trend

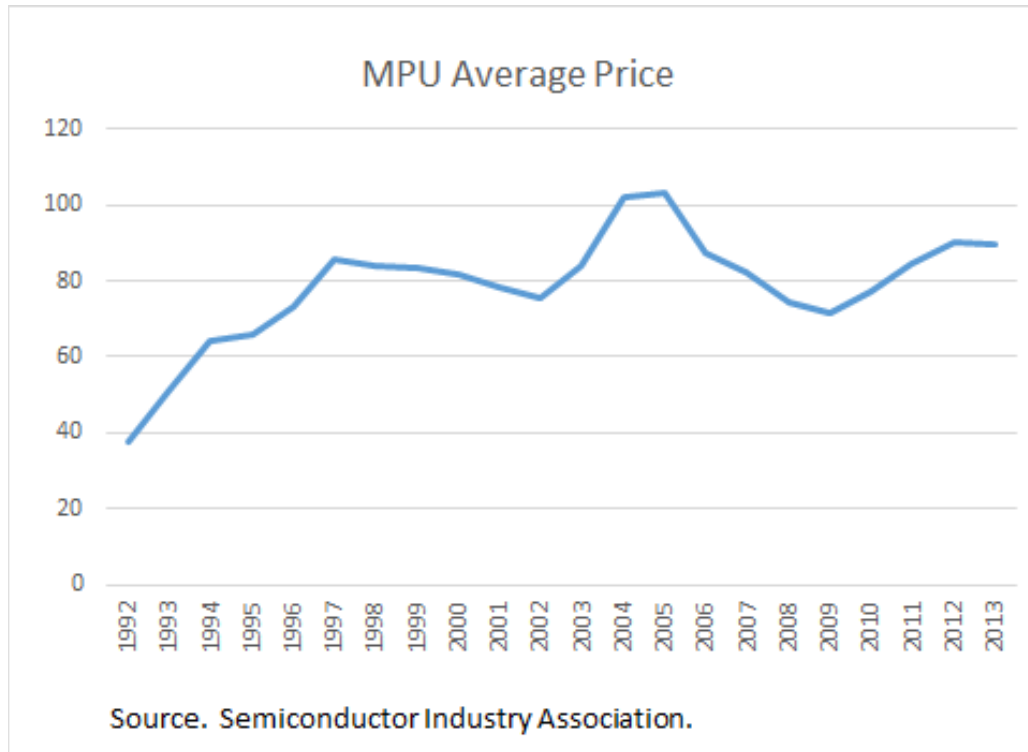
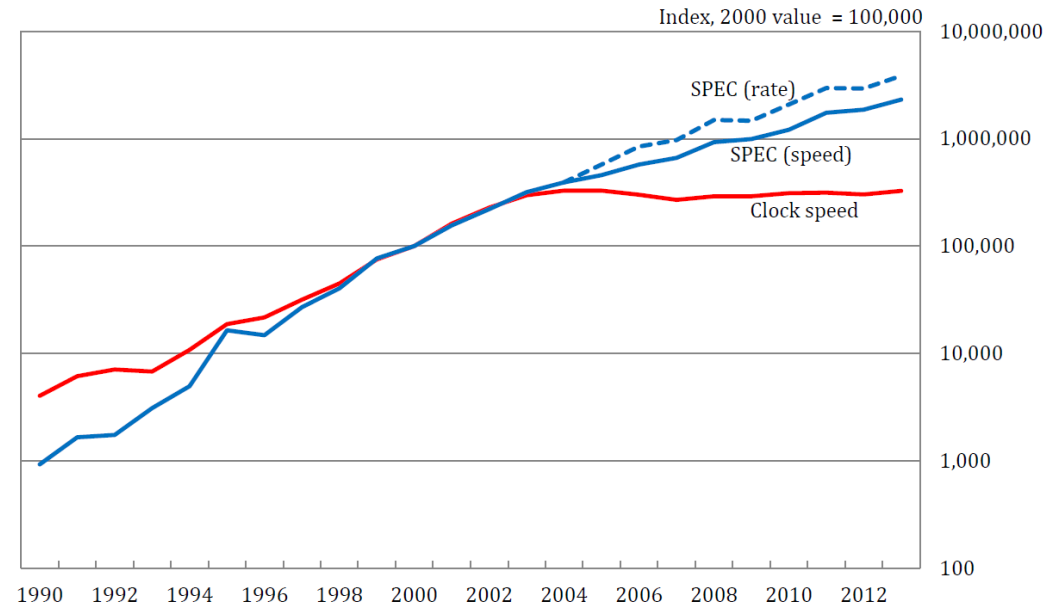


Figure 1: Desktop MPU Performance Measures



Source. Authors' calculations using data provided by Unni Pillai and performance information from Intel price lists and SPEC corporation.

Plausibility check: Average prices are largely flat and performance continues to climb...  
suggesting price-performance ratios continue to fall rapidly.

Four possible explanations for this contradiction between the PPI and “aggregate price-performance ratio”



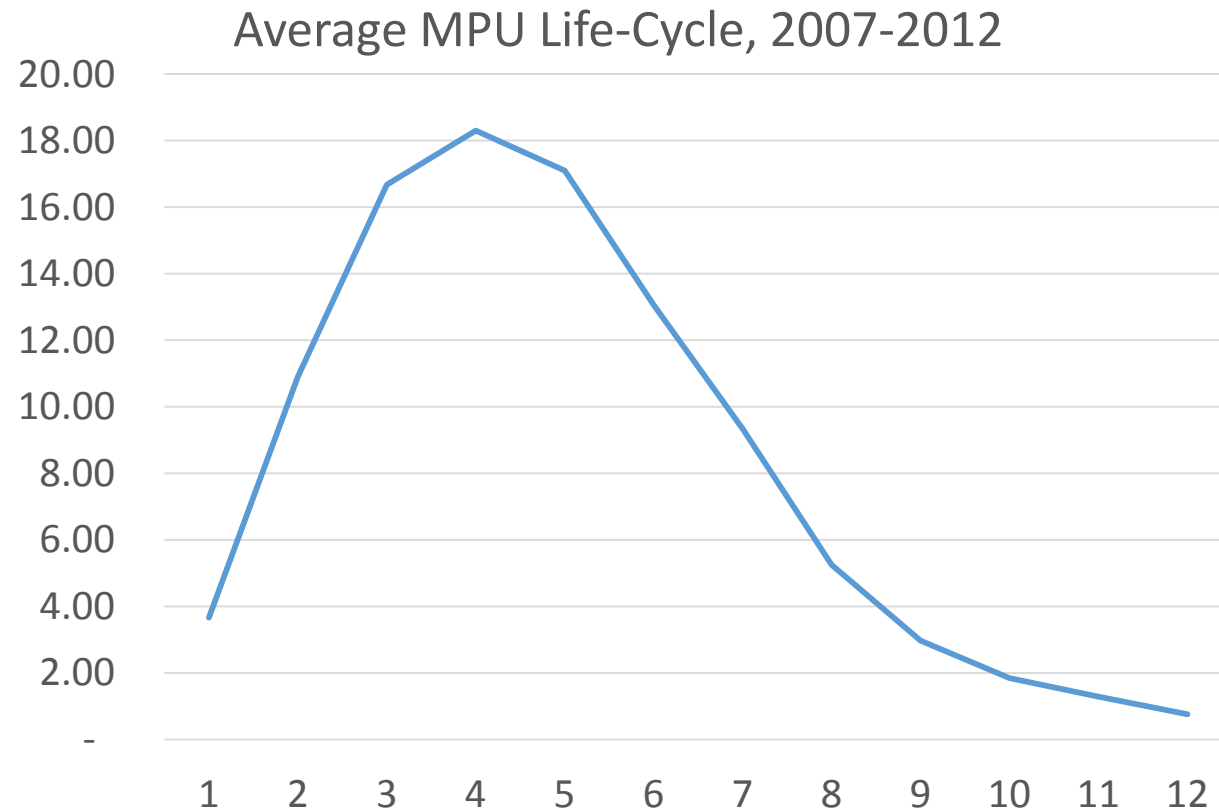
# Explanation 1: Benchmarks are Hype

<u>Selected SPEC Consortium Members</u>		
<u>Processor Companies</u>	<u>Major Customers</u>	
Intel	Acer Inc.	Hitachi Ltd.
Advanced Micro Devices	Amazon Web Services	HP Inc.
IBM	Apple Inc.	Lenovo
	Dell, Inc.	Microsoft
ARM	Fujitsu	NEC - Japan
NVIDIA		
Qualcomm Technologies Inc.		

- Some industry observers are skeptical of benchmarks, but
- Both producers and customers are in on the benchmark design.
- Also they are widely employed by academics.
- So, who are they trying to fool?
  
- **Benchmarks are hype? Answer: No.**

# Explanation 2: Vestigial Prices?

- Overpriced old chips remain on the list but nobody buys them?



Source. Author's calculations from NPD data.

- Average PC MPU life cycle is about 6 quarters.
- **Vestigial prices? Answer: No.**
- *Note that the unit pattern documented in Sawyer and So is based on MDR/Instat. Units in that database are made up using a model.*

# Explanation 3: Unseen Discounts

- PC industry is maniacal about squeezing costs out of the supply chain. Would they pay the same price for an inferior chip?

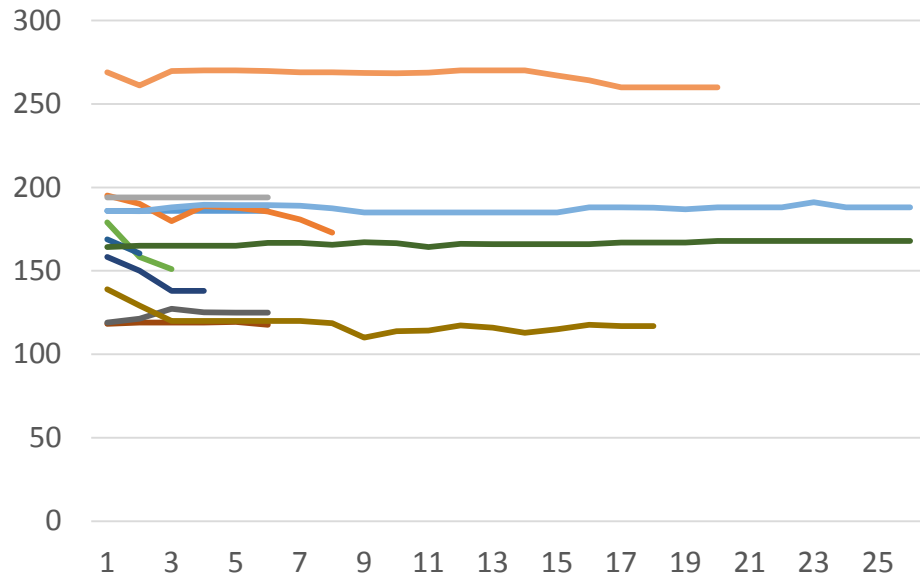
## State of New York v. Intel, No. 1:09-cv-00827 (D. Del. 2009)

- 2006: Dell offers PCs with AMD processors.
- Craig Barrett email to Paul Otellini:  
“Stop writing checks immediately and **put them back on list prices asap.**”

- **Unseen discounts? Answer: Yes.**
- *But we don't know enough detail to adjust prices.*

# Explanation 4: List Price is for Suckers

Core 2 Duo Retail Prices  
2012-2013



Source. Sharkey Extreme website.

## MPU accounting, 2011

- 371 PC MPUs sold
- 364 million PCs sold
- 7 million MPUs unaccounted for
- 1% of the global MPU market

Source. IDC, Inc. market trackers.

- Do retail customers pay the flat list prices? Yes.
- Are there a lot of retail customers? No.

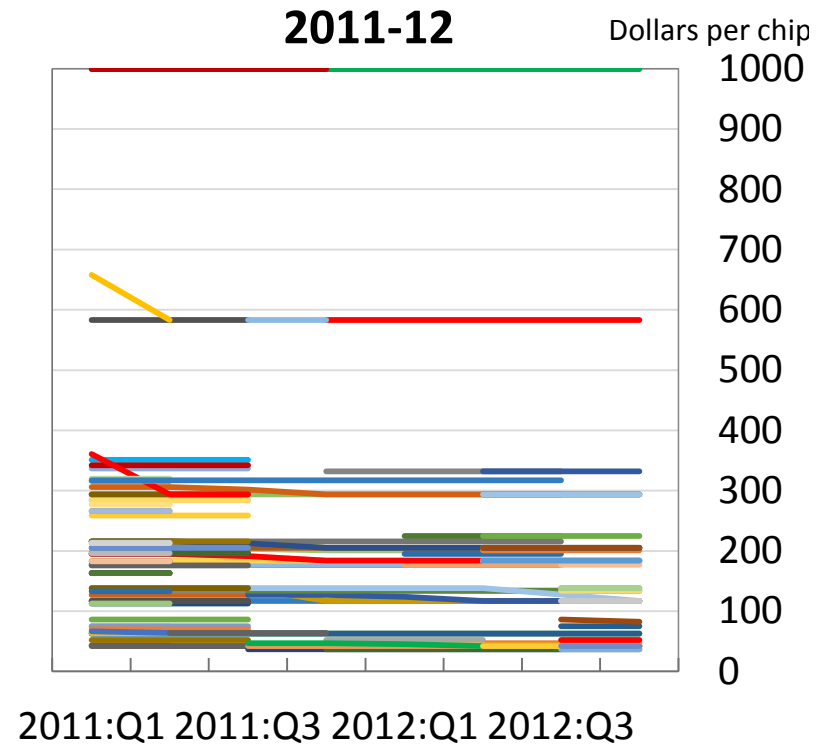
# Sticky List Price Explanations: Summary

- Benchmarks are hype? No.
- Late product cycle volumes are trivial? No.
- Unseen discounts? Yes.
  - ... but nobody knows the details except Intel.
- Some customers pay list? Yes.
  - ... but the market is small.
- This is a thorny measurement problem with no perfect solution.

# What to do? Matched Model Indexes

## Four BLS quality adjustment methods

1. Premium = all quality
2. Premium = all inflation
3. Use class mean
4. Explicit quality adjustment



First three methods will not work when entering price premium = 0.

Fourth method will require QA to exceed the (zero) price premium. Against BLS practice.

Matched model indexes won't work.

# What to do? Hedonics

- Time dummy approach is **NEW**, for BLS.
- (Hedonics used for computers are cross-sectional.)
- Avoids the “intuitive coefficients” interpretation trap: characteristics function as control variables. (See Pakes)
- Choice of matched model or hedonics is dictated by the characteristics of the data.
- ***In this case***, hedonics is a better approach.

# Which Prices to Use?

- Two types of price-quality covariation
  - Type 1, holding life-cycle fixed: meaningful.
  - Type 2, across life-cycle: polluted.
- The more type 2 variation you use, the flatter your hedonic price index will be.
- Not just a question of life-cycle length.

## Solutions

- Use only entry prices. (Gordon, 1989)
- “Leading edge” dummy. (Dulberger et al., 1986)



# What Control Variables to Use?

- Answer: controls that affect **both** user value and production cost
- Benchmark scores.
- Power consumption.
- Alternatively: a set of engineering features that affect performance. (See Chwelos)
- Not both: identifying coefficients using performance *conditional on* engineering features, which is non-linear or idiosyncratic.

# Estimation methodology

Some things to think about / issues where I found the exposition to be weak.

- Overfitting?
- What data generating process do the authors have in mind? The dataset is the population, not a sample.
- Relatedly, is this fundamentally an index number problem rather than a statistical problem?
- Abdicating role of industry knowledge? Hedonic specification is fundamentally structural.
- Public relations issue? Will the public “swallow” this methodology?

# Questions/Requests for BLS

- Will this be implemented for import and export prices as well?
- Please publish the regression results.  
(And for computers!)
- Why not ask the computer companies what price they're paying for MPUs?
- (We need an input price index program!)

# Conclusion

- **A great new direction for BLS.**
- **An admirable effort to tackle a thorny measurement problem.**

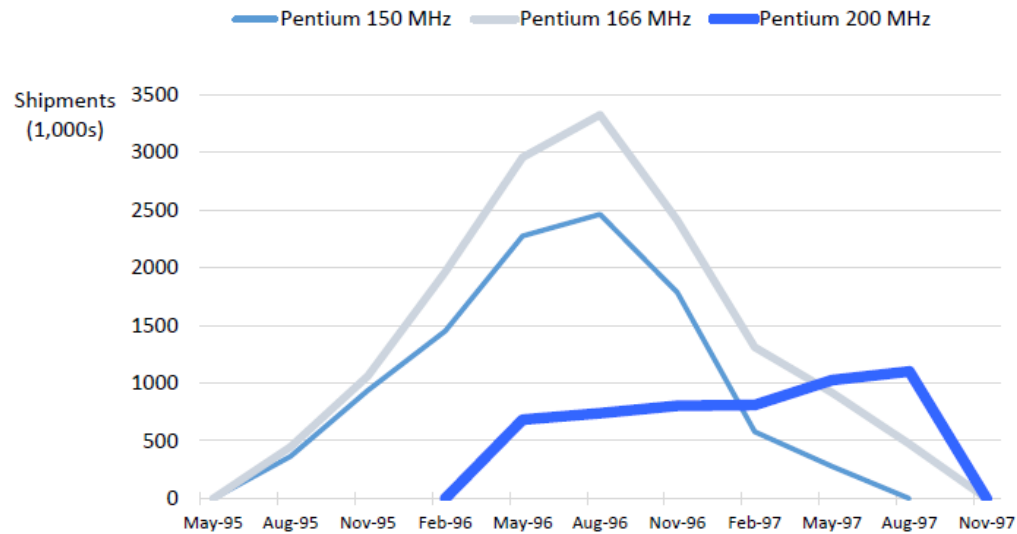
# Reference Slides

# References

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- **Doms, Mark, Ana Aizcorbe, and Carol Corrado.** 2003. "When do Matched-Model and Hedonic Techniques Yield Similar Measures?" (2003-14). FRS San Francisco working paper.
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- **Flamm, Kenneth.** 2007. "The Microeconomics of Microprocessor Innovation" University of Texas working paper.
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- **Holdway, Michael.** 2000. "An Alternative Methodology: Valuing Quality Change for Microprocessors in the PPI." BLS working paper.
- **Pakes, Ariel.** 2003. "A Reconsideration of Hedonic Price Indexes with an Application to PC's" *American Economic Review*, 93(5): 1578-1596.

# Instat/MDR MPU Database

Figure 2: Intel Microprocessor Shipments<sup>26</sup>



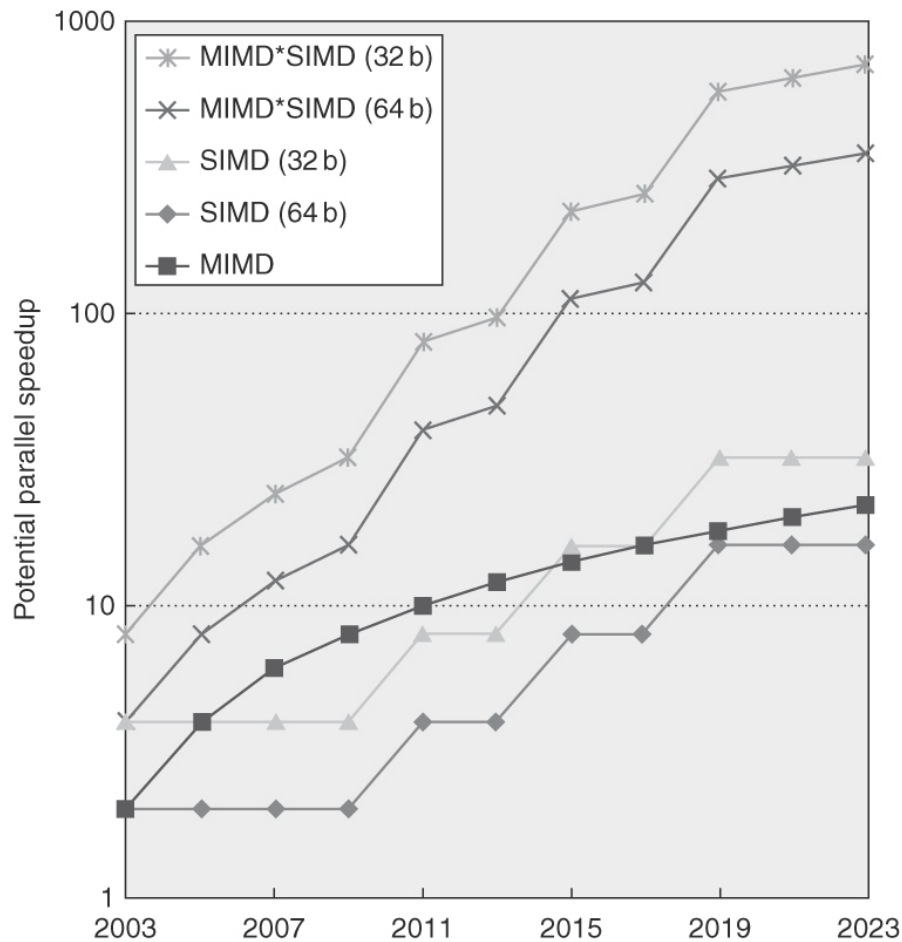
- Unit shipments are “modelled”

*“the Intel Service model predicted shipments by overlaying a **Guassian [sic] curve on the price points** for the various SKUs. Each new processor SKU was given a ramp up and ramp down shipment curve as well. The aggregate of the model for units and revenue was then compared with financial reports from Intel. If necessary, the model was hand tweaked to fit Intel disclosures.”*

Kevin Krewell,

(personal email 8/21/2012):

# Potential performance improvement from parallelization



**Figure 4.1 Potential speedup via parallelism from MIMD, SIMD, and both MIMD and SIMD over time for x86 computers.** This figure assumes that two cores per chip for MIMD will be added every two years and the number of operations for SIMD will double every four years.

Roughly +0.23 log points per year.



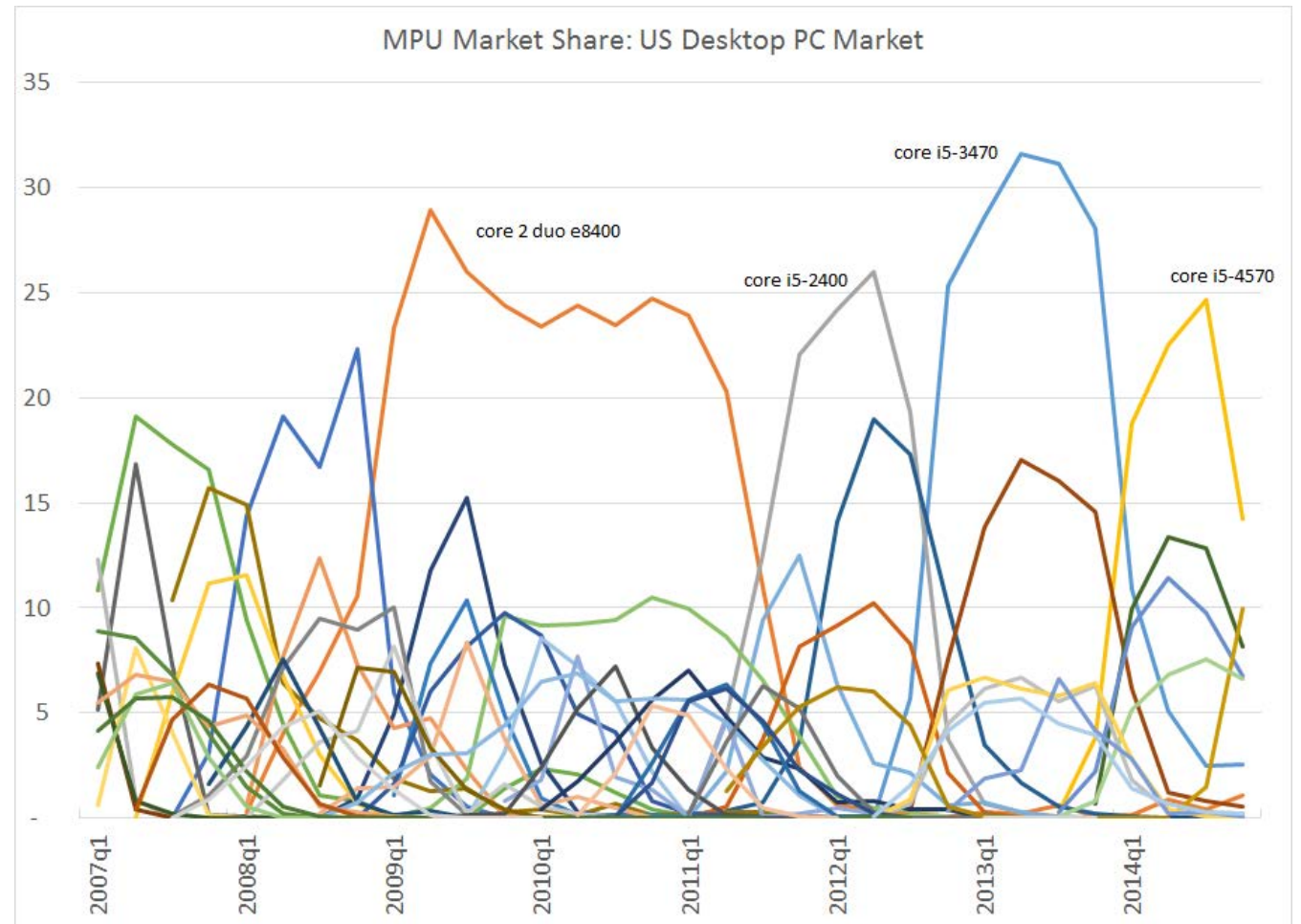
# Weights matter in the cross-section

Which price observations to use?

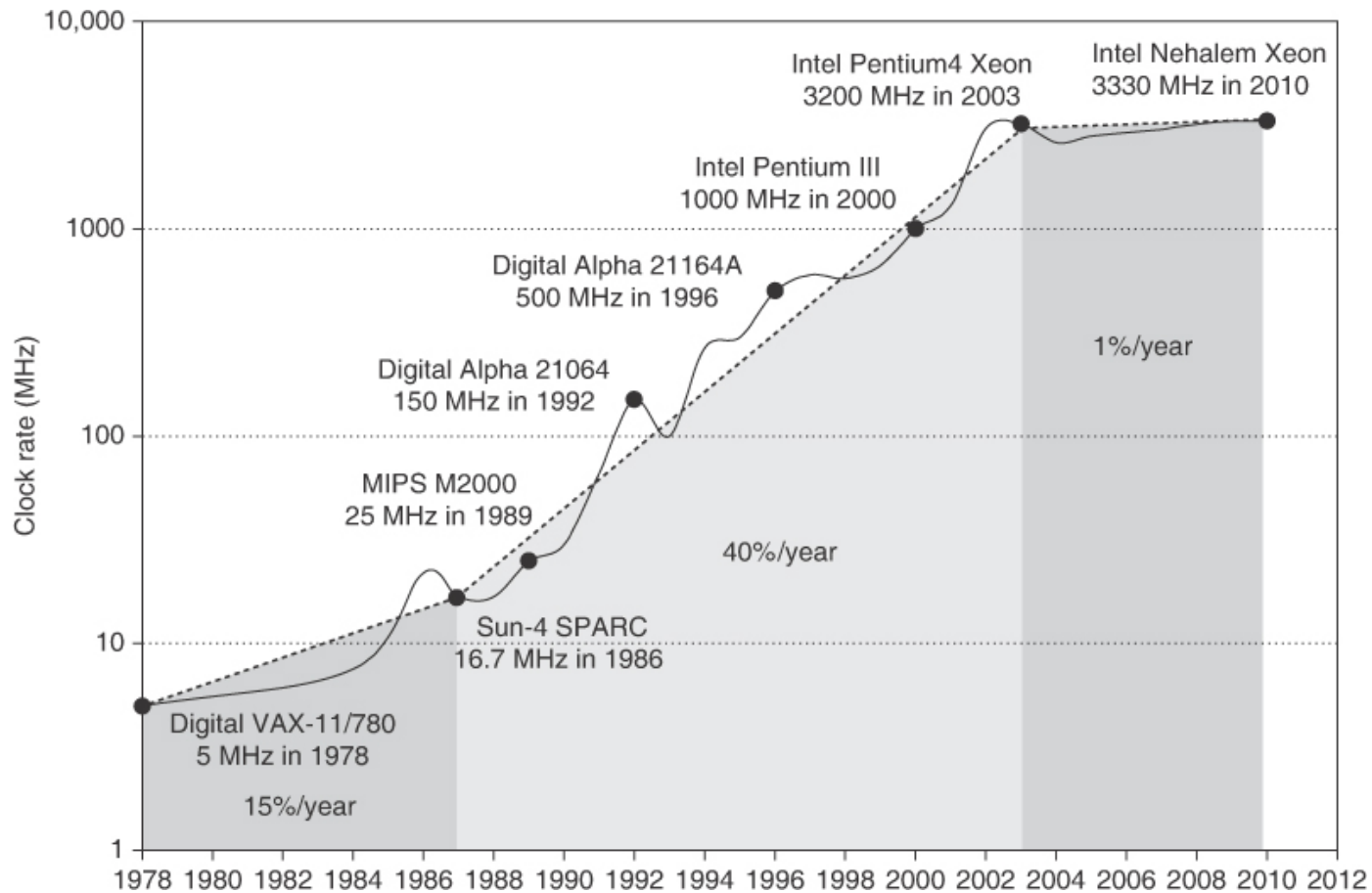
Table summarizing Life Cycle market share  
Density and quarter choice

More important: Which models to use?

Price index using the MPUs that reach  
5% ever? 1% ever?



# Slowdown Explanation 1: Stalled Clockspeed



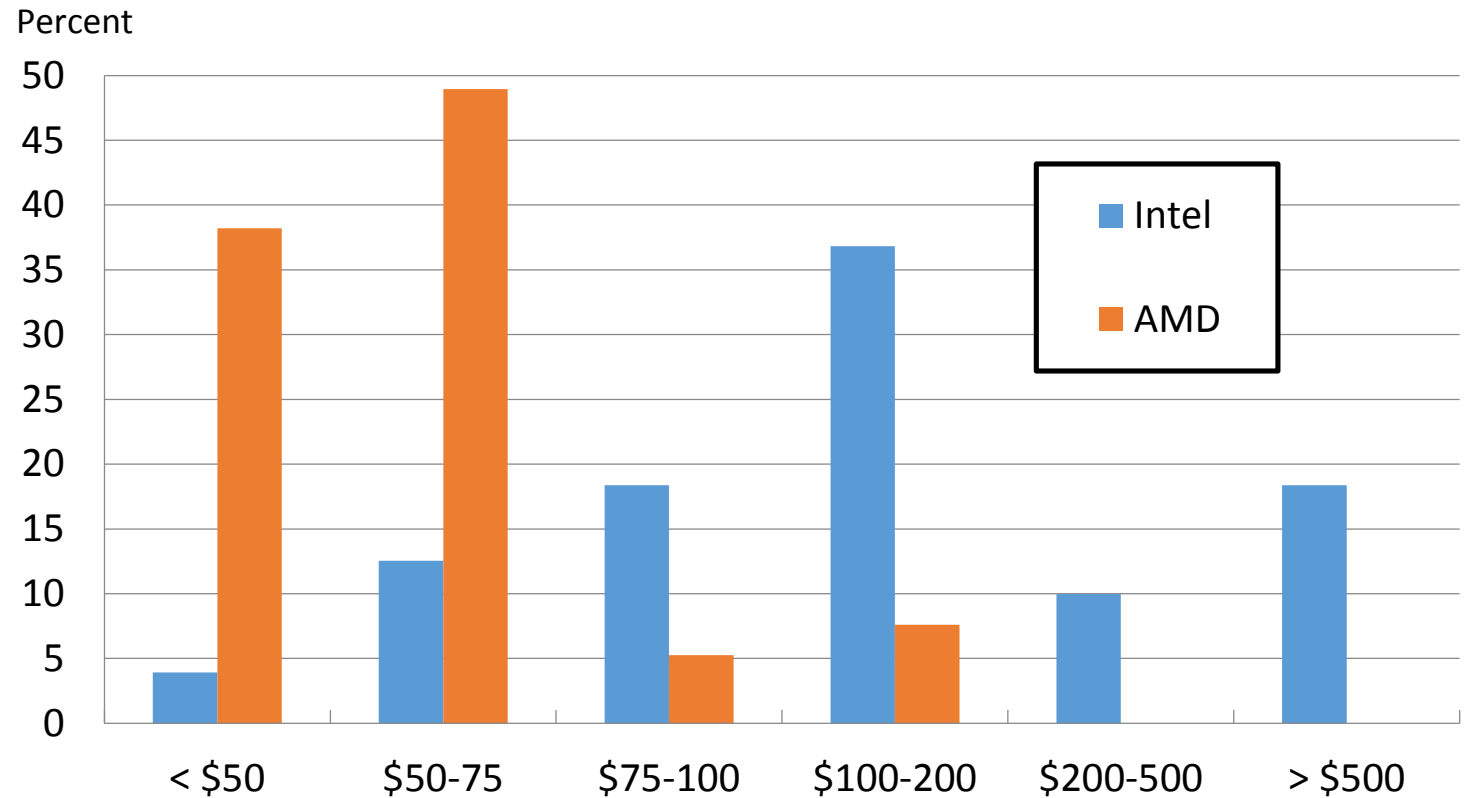
**Figure 1.11 Growth in clock rate of microprocessors in Figure 1.1.** Between 1978 and 1986, the clock rate improved less than 15% per year while performance improved by 25% per year. During the “renaissance period” of 52% performance improvement per year between 1986 and 2003, clock rates shot up almost 40% per year. Since then, the clock rate has been nearly flat, growing at less than 1% per year, while single processor performance improved at less than 22% per year.

# Market Structure

Starting in 1997, AMD was a close competitor to Intel for leading edge technology

2006: with Core 2 Duo / Pentium M, Intel seized the high end of the market.

## Compute MPU Price Distribution, 2013



Note. Data cover 2013:Q1 through 2013:Q3.

Source. Authors' calculations based on data from IDC Research, Inc.